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APPLICATION FOR PATENT

FOR INVENTION OF

GENERATING ADJUSTABLE-DELAY CLOCK SIGNAL FOR PROCESSING COLOR SIGNALS

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GENERATING ADJUSTABLE-DELAY CLOCK SIGNAL FOR PROCESSING COLOR SIGNALS

1. Field of the invention.

The present invention is related to the field of generating signals for displays, and more specifically to circuits, devices, and methods for generating a clock signal having a delay suitable for processing a color signal.

2. Background.

Color displays frequently display color data that is in digital form. The color data is usually available in color signals that are in analog form. An interface for processing color signals typically employs an Analog to Digital Converter (ADC), for converting the available analog color signals into digital data suitable for displaying. Conversion is improved if it occurs at a moment in time that is long enough after the received color signal has settled to its final value, but not too long so as to delay operation of the whole system.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will become more readily apparent from the following Detailed Description, which proceeds with reference to the accompanying drawings, in which:

FIGURE 1 is a block diagram of an interface for processing color signals for a display;

FIGURE 2 is a time diagram showing a waveform of a received color signal, and windows within which an analog color signal may advantageously be sampled for being converted into a digital signal;

FIGURE 3 illustrates a sample schematic diagram of a circuit for implementing a Phase Locked Loop (PLL) circuit of the interface of FIGURE 1;

FIGURE 4 illustrates a phase diagram, and further how the phases of four phased signals and their negatives define eight sectors;

FIGURE 5 illustrates is a diagram of a sector of the phase diagram of FIGURE 4, further illustrating the relative location of a general requested delay;

FIGURE 6 illustrates a diagram of the sector of FIGURE 5, showing also simulated phases for representing a general requested delay;

FIGURE 7 illustrates a table of values of pairs of weights for embodying the simulated phases of FIGURE 6;

FIGURE 8 illustrates a block diagram of a phase adjuster that generates a delay signal from phased signals that are apart by an odd multiple of 45 degrees;

FIGURE 9 illustrates a schematic diagram of an embodiment of the phase adjuster of FIGURE 8 using Integrated Circuits (ICs);

FIGURE 10 illustrates a schematic diagram of a circuit for embodying a phase decoder of the phase adjuster of FIGURE 8;

FIGURE 11 illustrates a schematic diagram of a circuit for embodying two phase selectors of the phase adjuster of FIGURE 8;

FIGURE 12 illustrates a schematic diagram of a circuit for embodying a Phase Digital to Analog Converter (PDAC) of the phase adjuster of FIGURE 8;

FIGURE 13 illustrates a schematic diagram of a circuit for embodying a phase mixer of the phase adjuster of FIGURE 8; and

FIGURE 14 illustrates a flowchart for describing a method according to an embodiment of the present invention.

DETAILED DESCRIPTION

The present invention is now described. While it is disclosed in its preferred form, the specific embodiments of the invention as disclosed herein and illustrated in the drawings are not to be considered in a limiting sense. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Indeed, it should be readily apparent in view of the present description that the invention may be modified in numerous ways. Among other things, the present invention may be embodied as devices, methods, software, and so on. Accordingly, the present invention may take the form of an entirely hardware embodiment, an entirely software embodiment or an embodiment combining

software and hardware aspects. The following detailed description is, therefore, not to be taken in a limiting sense.

Throughout the specification, the meaning of "a," "an," and "the" may also include plural references. The meaning of "in" includes "in" and "on." The term "coupled" means a direct connection between the items that are connected, or an indirect connection through one or more intermediary devices or components.

Briefly, the present invention provides circuits, devices, and methods for providing a phase delay and using it to select when an analog color signal is processed. The phase delay is adjustable, which permits choosing a moment in time when the operation results in improved processing. A PLL circuit receives a synchronizing signal of the color signal, and generates phased signals. A phase adjuster generates an adjustable delay signal by mixing in suitable proportions two of the phased signals that are 45 degrees apart. The delay signal is used by an analog to digital converter, to adjust when exactly it is to be sampled.

The invention offers the advantage that it offers a delay signal with a fine resolution of available phase delays. Further, the circuit of the invention operates at higher frequency and lower supply voltage.

The invention is now described in more detail.

FIGURE 1 is a block diagram of an interface circuit 100, which is used to receive signals from a computer 110 and convert them for use by a display 120. A graphics card 140 in computer 100 encodes an image in signals Rin, Gin, Bin and HSYNC. Analog color signals Rin, Gin, Bin encode respectively the red, green, and blue color content of the pixels. Signal HSYNC encodes a horizontal synchronizing signal that is associated with color signals Rin, Gin, Bin, and more particularly identifies the beginning of a new line on the display.

Color signals Rin, Gin, Bin are received in interface circuit 100, and are processed. Processing includes converting to digital color signals Rout, Gout, Bout. Signals Rout, Gout, Bout can be made from 8 bits each, or a different number of bits. Signals Rout, Gout, Bout are received in display 120, where they cause the encoded image to be displayed. They may be 256-level Pulse Amplitude Modulated (PAM) at the pixel frequency rate.

Interface circuit 100 may be embodied in any number of ways. For example, it may be implemented by itself as a standalone unit, or as part of either computer 110 or display 120. It may be embodied as an integrated circuit, or as a card or other way to implement a circuit.

Interface circuit 100 includes a phase locked loop PLL circuit 150, which may be used to generate a signal replicating the pixel clock used in display 120. PLL circuit 150 may advantageously have four stages, which can generate at least four phased signals from signal HSYNC. The phased signals are input into a phase adjuster 160, which generates a delay signal DS. In one embodiment, delay signal DS acts as a replicated pixel clock of the clock that is used within display 120.

Three high-speed Analog to Digital Converters (ADCs) 172, 174, 176 receive respectively color signals Rin, Gin, Bin. ADCs 172, 174, 176 process the received color signals Rin, Gin, Bin as controlled by the delay signal DS.

FIGURE 2 shows a waveform of a received one of color signals Rin, Gin, Bin. Each pixel is received over a time interval Tp. Within each time interval Tp, there is a window Tw for preferred sampling, to improve accuracy. Both the pixel time intervals Tp and the windows Tw are short. For example, the UXGA standard for high speed flat panel displays requires a pixel clock rate of 202 MHz. Thus the pixels have a time interval Tp of only 5ns. A portion of that is the time window Tw in which to be sampled accurately.

FIGURE 3 illustrates a sample schematic diagram of a circuit 300 for implementing phase locked loop (PLL) circuit 150. A frequency/phase detector 310 receives signal HSYNC, and a divided down signal clk_{VCO}/M. Detector 310 compares these two signals, and generates an output that is directed to a charge pump 320, whose output is in turn directed to a filter 330. An output of filter 330 is directed to a fast clock generator 340, which is made from a voltage to current converter and a current controlled oscillator. Fast clock generator 340 outputs four phased signals p45, p90, p135 and p180. Each of these signals may optionally be provided with its positive (p) sign, and also be provided with its negative sign (n). One more output carries fast clock signal clk_{VCO}, which may be just one more of the clock phases. A divide-by-M counter 350 receives fast clock signal clk_{VCO}, and generates divided down signal clk_{VCO}/M.

FIGURE 4 is a phase diagram given as a circle that represents time interval Tp. Four phased signals have phases P1, P2, P3 and P4, at angles that are 45, 90, 135, and 180 degrees respectively. Their negatives have phases P5, P6, P7 and P8, at angles that are -45, -90, -135, and -180 degrees respectively. All phases P1, ..., P8 define eight sectors S1, ..., S8 between them in the circle.

To implement a general required delay, its location may be found first in a phase diagram, such as that of FIGURE 4. Then two phased signals may be chosen, such that they define between them a sector on the phase diagram, which encompasses the general required delay. As an example only, a general requested delay RD is found within sector S1, bordered by phases P1 and P2. Within that sector, general requested delay RD has a phase angle α measuring counterclockwise from phase P1.

FIGURE 5 is a diagram of sector S1 of the phase diagram of FIGURE 4, further illustrating the relative location of a general requested delay. Sector S1 was chosen because it encompasses general requested delay RD. For the diagram of FIGURE 5, sector S1 was chosen to have an angle of 45 degrees, as is preferred, although other multiples could be used, for example odd multiples of 45 degrees.

The sector is encompassed by phases P1 and P2, as determined in FIGURE 4. Then the phase signal that has phase P1 is multiplied with a first preselected weight a, shown as a vector in FIGURE 4. And the phase signal that has phase P2 is multiplied with a second preselected weight b, also shown as a vector in FIGURE 4. Then the first and second multiplied phased signals are added together as vectors, to reconstruct the general requested delay. The phase angle α of general requested delay RD has a certain trigonometric relationship with weights a and b.

The above was performed for a general requested delay RD. In the practice of the invention, it is acceptable to simulate the general requested delay within the sector by a simulated phase. The first and second weights are selected so that simulated phases are used. When a delay is chosen of delay signal DS, it is expressed in terms of one of the simulated phases, as described below.

FIGURE 6 is a diagram of the sector of FIGURE 5, where general requested delay RD is shown. Further, the invention includes simulated phases M1, M2, M3,

spaced within sector S1 at even intervals of 11.25 degrees. As can be seen in FIGURE 6, the general requested vector RD can best be simulated by phase M3.

FIGURE 7 illustrates a table 700 of values of pairs of weights a and b. According to a set 1, the pairs of values of a and b have a sum total weight of 16. According to a set 2, the pairs of values of a and b have a sum total weight of 4. Set 1 is merely a multiple of set 2 by a multiplication integer. In advantageous embodiments of the invention, once weight a is known, weight b is found by subtraction from the sum total weight. It will be observed that, in set 2, weight a takes one of the values of zero, one, two, three and four.

FIGURE 8 is a block diagram of a phase adjuster 800. Phase adjuster 800 generates a delay signal DS from phased signals p45, p90, p135, p180 and their negatives, which are also shown in FIGURE 4. Phase adjuster 800 includes a first phase selector 810, a second phase selector 820, a phase mixer 830 and a phase decoder 840.

First phase selector 810 selects a first one of phased signals p45, p90, ..., designated as phase a. Second phase selector 820 selects a second one of phased signals p45, p90, ..., designated as phase b. Phase a and phase b are input into phase mixer 830. Phase mixer 830 multiplies the first selected phased signal with first weight a, and the second selected phased signal with second weight b. Phase mixer 830 then adds the first and the second multiplied phased signals to derive delay signal DS. In other words, DS=a*phase a + b* phase b.

Phase selectors 810 and 820 select phases by receiving phase selection signals. In some embodiments, some of the phase selection signals are received into the phase mixer, for example an inverted signal. In yet other embodiments, redundant signals are used to facilitate switching values.

The phase selection signals may originate from decoder 840. Decoder 840 may decode a phase adjust signal PA, and use it to generate the individual phase selection signals, as per the above. In some embodiments, phase adjust signal PA simply steps through successive values, seeking to optimize the overall result.

Phase adjuster 800 further includes a Phase Digital to Analog Converter (PDAC) 860. In some embodiments, PDAC 860 is implemented as part of phase mixer 830. PDAC 860 generates a first weight signal encoding the first weight a, and a second weight signal encoding the second weight b. The first and the second weight signals are

received in phase mixer 830 to derive delay signal DS. In the embodiment of FIGURE 8, decoder 840 also generates weight selection signals that are received in PDAC 860. These weight selection signals are used to generate the first and second weight signals.

FIGURE 9 is a schematic diagram of a circuit 900 for embodying phase adjuster 800 using Integrated Circuits (ICs). A phase selector IC 910 implements phase selectors 810 and 820, and a phase mixer IC 930 implements phase mixer 830. A phase decoder IC 940 implements decoder 840, and a PDAC IC 960 implements PDAC 860.

FIGURE 10 is a schematic diagram for embodying phase decoder 840 of FIGURE 8. Selection signals are generated for other components.

FIGURE 11 is a schematic diagram of a circuit 1100 for embodying phase selectors 810, 820 of phase adjuster 800. Circuit 1100 may well be a circuit within integrated circuit 910.

FIGURE 12 is a schematic diagram of a circuit 1200 for embodying a Phase Digital to Analog Converter (PDAC) 860 of phase adjuster 800. Circuit 1200 includes a first current source M39 that draws a first current. The first current, by its value, encodes or represents the first weight a for the phase mixer. Circuit 1200 also includes a second current source M41 that draws a second current. The second current, by its value, encodes or represents the sum total weight of weights a and b. Circuit 1200 moreover includes a third current source M40 that draws a difference current between the second current (through M41) and the first current (through M39). The difference current is used to derive the second weight signal. Indeed, the current sources are implemented by transistors. Transistor M39 activates transistor M22, whose current is mirrored by transistor M26, and whose current is output by transistor M32. And transistor M40 activates transistor M20, whose current is mirrored by transistor M24, and whose current is output by transistor M29. The design is repeated for current sources M16, M19. The latter are made to appropriate scale, for implementing the values of the weights table 700. For example, transistor M41 is made the same size as transistor M16, and transistor M19 is made twice the size of M41. These components may be made to draw very small currents.

FIGURE 13 is a schematic diagram of a circuit 1300 for embodying a phase mixer of phase adjuster 800. Circuit 1300 receives signals from the other components and outputs delay signal DS.

FIGURE 14 is flowchart 1400 illustrating a method according to an embodiment of the invention. The method of flowchart 1400 may be practiced by different embodiments of the invention, including but not limited to interface 100, circuit 800, and circuit 900.

Moving from a START block, the process advances to block 1410, where a synchronizing signal is received, that is associated with a color signal. At a next block 1420, phased signals are derived. At a next block 1430, two of the phased signals are selected, which have a phase difference of an odd multiple of approximately 45 degrees. At a next block 1440, first and second weights are selected. One of them may be selected by subtracting the other one from a known sum total. At a next block 1450, the first phased signal is multiplied by the first weight, and the second phased signal is multiplied by the second weight. At a next block 1460, the multiplied signals are added together to derive a delay signal. At next block 1470, the delay signal is used to control the analog to digital conversion of the color signal. Then the process may perform other actions.

Numerous details have been set forth in this description, which is to be taken as a whole, to provide a more thorough understanding of the invention. In other instances, well-known features have not been described in detail, so as to not obscure unnecessarily the invention.

The invention includes combinations and subcombinations of the various elements, features, functions and/or properties disclosed herein. The following claims define certain combinations and subcombinations, which are regarded as novel and non-obvious. Additional claims for other combinations and subcombinations of features, functions, elements and/or properties may be presented in this or a related document.